HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

12936A

PRIVILEGED INTERRUPT FENCE ACCESSORY

(FOR 2100 COMPUTERS)

Printed-Circuit Assembly:

12936-60001, Series 1353

12936-90001

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

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1. INTRODUCTION.

2. This manual provides general information, installation, theory of operation, maintenance, and replaceable parts information for the HP 12936A Privileged Interrupt Fence.

3. GENERAL DESCRIPTION.

4. The HP 12936A Privileged Interrupt Fence provides a means to distinguish between privileged (high priority/low select code) and non-privileged (low priority/high select code) I/O devices in both DOS-III revision B and RTE systems.

5. The HP 12936A Privileged Interrupt Fence consists of the following:

a. One privileged interrupt fence printed-circuit assembly (PCA), part no. 12936-60001.

b. One Installation and Service Manual, part no. 12936-90001.

c. One Privileged Interrupt Fence Diagnostic tape, part no. 12936-16001.

6. The privileged interrupt fence is a single printed-circuit assembly which is installed in one of the I/O slots in an HP 2100A or an HP 2100S Computer mainframe to provide a programmable I/O barrier between high and low priority devices. It contains the circuitry to control both the generation of interrupts and to inhibit the priority line to lower priority devices under program control.

7. SPECIFICATIONS.

8. Specifications for the HP 12936A Privileged Interrupt Fence are provided in table 1.

Table 1. Privileged Interrupt Fence Specifications

CURRENT (SUPPLIED BY COMPUTER)	
-2V supply	30 mA
+5V supply	300 mA
LOGIC VOLTAGE LEVELS	
Logic 1 (high)	+2.4V or greater
Logic 0 (low)	+0.4V or less
DIMENSIONS	
Width	7-3/4 in. (19.7 cm)
Height	8-11/16 in. (22.1 cm)
WEIGHT	
Net Weight	9 oz (0.255 kg)
Shipping Weight	2 lbs (0.907 kg)

9. SUPPORTING DOCUMENTS.

10. Documentation pertinent to proper operation of this accessory is listed in table 2.

Table 2. List of Supporting Documents

MANUAL TITLE	PART NUMBER
DOS-III Disc Operating System Manual*	02100-90136
RTE Programming and Operating Manual	02005-90002
HP 2100 Series Diagnostic Configurator	02100-90157
Basic Binary Loader – Basic Binary Disc Loader – Basic Moving Head Disc Loader	5951-1376

*June 1973 edition with Update Package 1 dated March 1974.

11. UNPACKING AND INSPECTION.

12. If this accessory is received separate from the computer, inspect the shipping carton for damage before opening. If external damage is evident or if the carton rattles, request that the carrier's agent be present when the contents of the accessory are unpacked. Inspect the contents for damage (cracks, broken parts, etc.). If the contents are damaged and fail to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. Sales and Service Offices are listed at the back of this manual. Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged components without waiting for any claims against the carrier to be settled.

13. IDENTIFICATION.

14. Hewlett-Packard uses five digits and a letter (00000A) to identify standard accessories. If the designation of the accessory received does not agree with the designation on the title page of this manual, there are differences between the accessory received and the accessory described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office. These offices are listed at the back of this manual.

15. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code stamped below the part number on the PCA. The letter identifies the revision of the etched trace pattern on the unloaded board. The series code (middle four digits) refers to the electrical characteristics of the loaded PCA and to the positions of the components. If the series code stamped on the PCA does not correspond exactly with the series code printed on the title page of this manual, the PCA differs from the one described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the PCA.

16. INSTALLATION.

17. If the privileged interrupt fence is received separate from the computer, install it as follows:

a. Turn off power at the computer.

b. Remove the top access cover from the computer.

c. Insert the privileged interrupt fence into the I/O slot that corresponds to the desired select code between privileged (lower select code) and non-privileged (higher select code) devices.

Note: See the *DOS-III Disc Operating System Manual*, part no. 02100-90136 with Update Package 1 for further information regarding device priority.

18. INSTALLATION CHECKOUT.

19. Turn on power at the computer, then perform the diagnostic tests outlined in the HP 12936 Privileged Interrupt Fence Diagnostic which is contained in the appendix A, located at the back of this manual. If the diagnostic tests are completed without an error halt, the privileged interrupt fence is operating correctly. The top access cover may then be replaced. If the diagnostic tests indicate an error, perform the diagnostic troubleshooting procedure outlined in paragraph 39.

20. THEORY OF OPERATION.

21. The circuitry of the privileged interrupt fence is comprised of four flip-flops and associated gating logic. These flip-flops, namely the Flag Buffer, Flag, Control, and IRQ flip-flops, control each of the four operating states. These states are illustrated in figure 1 and discussed in the following paragraphs. See the schematic diagram (figure 6) during these discussions. Timing information is provided in figure 2. Signal mnemonics are defined in table 3.

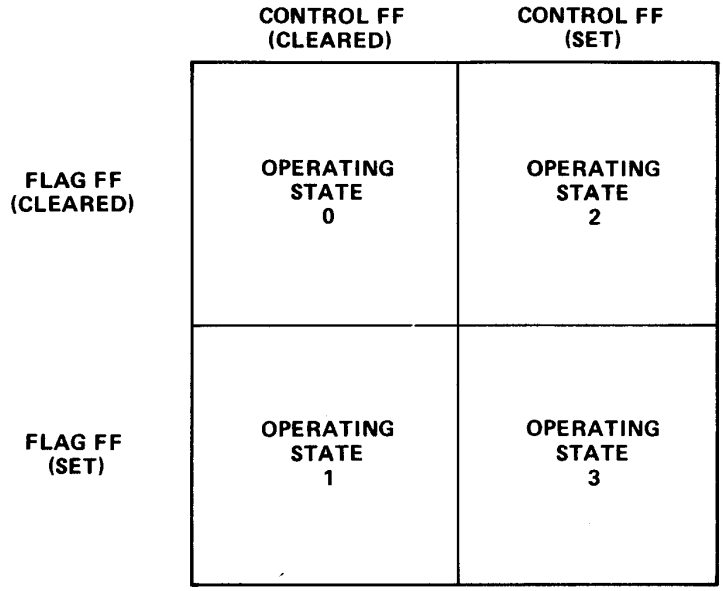
22. OPERATING STATE 0

23. Operation in this state occurs when the fence is initialized at time T5 by high POPIO and CRS signals. These signals go high when power is first applied or when the EXTERNAL PRESET switch on the operator panel is pressed. When high, POPIO and CRS clear the Flag Buffer, Flag, Control, and IRQ flip-flops. These flip-flops may be at either state when the privileged interrupt fence is initialized. With the Flag and Control flip-flops cleared, the priority line (PRL) to lower priority devices (higher select codes) becomes high once the interrupt system is enabled, ie, when IEN and PRH are both high. This will permit devices with a lower priority to request an interrupt.

24. The FLG and IRQ signals from the privileged interrupt fence will be low because the IRQ flip-flop is cleared. It cannot be set by SIR at the next time T5 because the Flag Buffer and Flag flip-flops are both cleared. Operation will remain in this state until one of the I/O instructions that affect this PCA is programmed. A list of these I/O instructions as well as all other signals affecting the privileged interrupt fence is provided in table 3.

25. OPERATING STATE 1.

26. Operation in this state occurs when an OTA/B I/O instruction is programmed. Whenever an I/O instruction is programmed, IOG, SCL, and SCM will go high. These signals are "anded" to provide an I/O instruction enabling signal on the PCA. The OTA/B I/O instruction also causes IOO to go high during time T3T4. This sets the Flag Buffer flip-flop which in turn sets the Flag flip-flop at the next time T2, ie, when ENF goes high. With the Flag flip-flop set, the priority line (PRL) to lower priority devices goes low. This will prevent devices with a lower priority from requesting an interrupt. The priority line will remain low until the Flag flip-flop is cleared by programming a CLF I/O instruction.



OPERATING STATE 0

- FLAG FF AND CONTROL FF CLEARED
- FENCE OFF
- PRL HIGH (Permits lower priority devices to request an interrupt when IEN and PRH are both high)
- NO INTERRUPT REQUEST GENERATED (FLG and IRQ low)

OPERATING STATE 1

- FLAG FF SET AND CONTROL FF CLEARED
- FENCE ON
- PRL LOW (Prevents lower priority devices from requesting an interrupt)
- GENERATES AN INTERRUPT REQUEST (FLG and IRQ high when IEN and PRH are both high)

OPERATING STATE 2

- CONTROL FF SET AND FLAG FF CLEARED
- FENCE ON
- PRL LOW (Prevents lower priority devices from requesting an interrupt)
- NO INTERRUPT REQUEST GENERATED (FLG and IRQ low)

OPERATING STATE 3

- CONTROL FF AND FLAG FF SET
- FENCE ON
- PRL LOW (Prevents lower priority devices from requesting an interrupt)
- NO INTERRUPT REQUEST GENERATED (FLG and IRQ low)

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Figure 1. Privileged Interrupt Fence Operating States

27. When SIR goes high at the next time T5, the IRQ flip-flop will be set provided that the interrupt system is enabled, ie, when IEN and PRH are both high. When set, both FLG and IRQ will simultaneously go high. They will toggle every time T2 until the interrupt request is acknowledged by the computer. The Control flip-flop remains cleared during this operating state.

28. When the computer is ready to handle the interrupt, it will generate IAK at time T6. This signal together with the set-side output from the IRQ flip-flop will clear the Flag Buffer flip-flop which will prevent the IRQ flip-flop from being set again when SIR goes high at the next time T5. At time T2, the IRQ flip-flop will be cleared by ENF. This also causes FLG and IRQ to go low.

29. OPERATING STATE 2.

30. Operation in this state occurs when an STC I/O instruction is programmed. Here too, IOG, SCL, and SCM will go high when the I/O instruction is programmed. They are "anded" to enable STC to set the Control flip-flop at time T4. When set, this flip-flop causes the priority line (PRL) to lower priority devices to go low. This prevents devices with a lower priority from requesting an interrupt. The priority line will remain low until the Control flip-flop is cleared by programming a CLC I/O instruction.

31. Unlike operating state 1, this state does not generate an interrupt request when SIR goes high at time T5. This is due to the fact that the inverted set-side output from the Control flip-flop prevents the IRQ flip-flop from being set. Also the Flag Buffer and Flag flip-flops remain cleared during this operating state.

32. OPERATING STATE 3.

33. Operation in this state occurs when the Control flip-flop is set as in operating state 2 and the Flag flip-flop is also set as in operating state 1. Whenever either or both flip-flops are set, the priority line (PRL) to lower priority devices goes low. This will prevent devices with a lower priority from requesting an interrupt. The priority line will remain low until both the Flag and Control flip-flops are cleared by programming a CLF and CLC I/O instruction, respectively.

34. An interrupt request will not be generated in this state when SIR goes high at time T5 since the inverted set-side output from the Control flip-flop prevents the IRQ flip-flop from being set.

35. PREVENTIVE MAINTENANCE.

36. Detailed preventive maintenance procedures and schedules are given in the computer system documentation. There are no separate preventive maintenance procedures to be performed on this accessory.

37. DIAGNOSTICS.

38. The privileged interrupt fence can be checked for proper operation by performing the diagnostic tests outlined in the HP 12936 Privileged Interrupt Fence Diagnostic which is contained in the appendix A located at the back of this manual.

39. TROUBLESHOOTING.

40. Troubleshooting the privileged interrupt fence is accomplished by performing the diagnostic tests and analyzing the error halts that occur as the tests are being run. At the completion of the diagnostic tests, the computer will halt with the contents of the Memory Data Register (102077_8) displayed in the Display Register. The diagnostic tests can be repeated by pressing the RUN switch. When an error is detected, Test 9 of the diagnostic (Scope Loop) may be programmed and the states of the Flag, Control, and IRQ flip-flops observed at TP2, TP3, and TP4, respectively. As can be seen in figure 3, each operating state can be observed as well. Note that the state of the IRQ flip-flop can only be observed at TP4 when the interrupt system is enabled, ie, when IEN and PRH are both high.

41. Program Test 9 (Scope Loop) as follows:

a. When the diagnostic tests are completed and the computer halts with 102077_8 displayed in the Display Register, load 001000_8 into the Switch Register.

b. Press EXTERNAL PRESET.

c. Press RUN. The computer will halt with 102075_8 displayed in the Display Register.

d. Load 001000_8 into the A-Register. This selects Test 9 (Scope Loop).

e. Clear the Switch Register.

f. Press EXTERNAL PRESET.

g. Press RUN. The computer will loop on Test 9.

h. Monitor TP2 (Flag FF), TP3 (Control FF), and TP4 (IRQ FF). The waveforms should be as shown in figure 3.

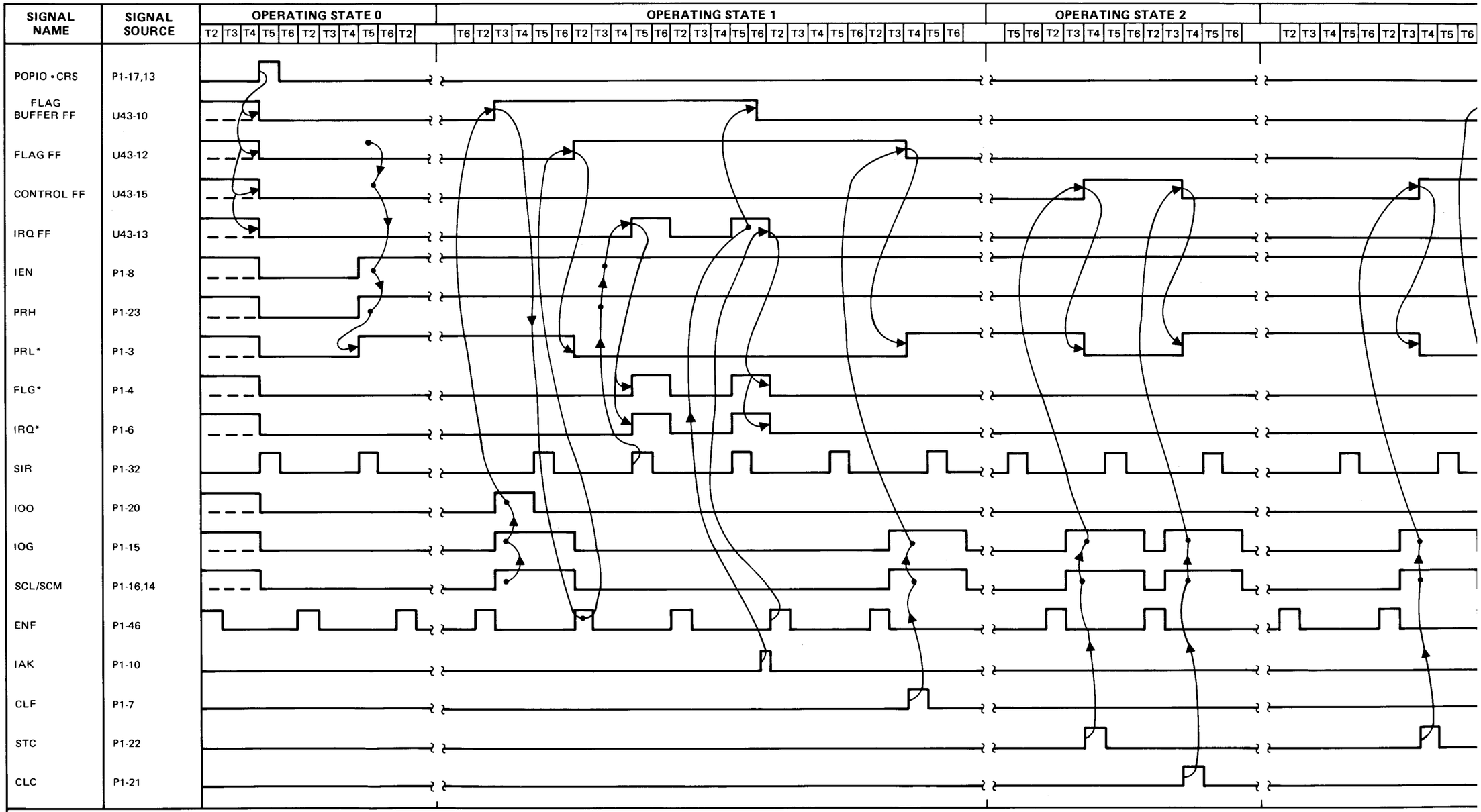
42. To further isolate a malfunction, refer to the integrated circuit, parts location, and schematic diagrams contained in figures 4 through 6. Table 4 lists the replaceable parts for the privileged interrupt fence.

Table 3. Privileged Interrupt Fence Signal List

MNEMONIC	SIGNAL NAME	FUNCTION
CLC*	Clear Control (I/O)	Clears the Control FF at time T4.
CLF*	Clear Flag (I/O)	Clears the Flag Buffer FF and Flag FF at time T4.
CRS	Control Reset (I/O)	Clears the Control FF at time T5.
ENF	Enable Flag (I/O)	Sets the Flag FF at time T2 if the Flag Buffer FF was previously set. Also clears the IRQ FF.
FLG	Flag	Signals generation of an interrupt request when the IRQ FF is set and the interrupt system is enabled.
IAK	Interrupt Acknowledge	Clears the Flag Buffer FF at time T6 in response to an interrupt request.
IEN	Interrupt Enable	Enables the interrupt system to lower priority devices. Also gates FLG and IRQ signals when the IRQ FF is set.
IOG	Input/Output Group	Provides an I/O instruction enabling signal at time T3T4T5T6 when "anded" with SCL and SCM.
IOO**	I/O Output	Sets the Flag Buffer FF at time T3T4.
IRQ	Interrupt Request	Requests an interrupt when the IRQ FF is set and the interrupt system is enabled.
POPIO	Power On Preset (I/O)	Clears the Flag Buffer FF, Flag FF, Control FF, and IRQ FF at time T5.
PRH	Priority High	Enables the priority line to lower priority devices. Also gates FLG and IRQ signals when the IRQ FF is set.
PRL	Priority Low	Permits lower priority devices to request an interrupt if high and the interrupt system is enabled. If low, it prevents lower priority devices from requesting an interrupt.
SCL	Select Code LSB	Provides an I/O instruction enabling signal at time T3T4T5T6 when "anded" with SCM and IOG.
SCM	Select Code MSB	Provides an I/O instruction enabling signal at time T3T4T5T6 when "anded" with SCL and IOG.
SIR	Set Interrupt Request	Sets the IRQ FF at time T5 if the Flag Buffer FF and Flag FF are set, the Control FF is cleared, and the interrupt system is enabled.
STC*	Set Control (I/O)	Sets the Control FF at time T4.

*I/O instruction.
**Generated by an OTA/B I/O instruction.

SIGNAL NAME	SIGNAL SOURCE
POPIO • CRS	P1-17,13
FLAG BUFFER FF	U43-10
FLAG FF	U43-12
CONTROL FF	U43-15
IRQ FF	U43-13
IEN	P1-8
PRH	P1-23
PRL*	P1-3
FLG*	P1-4
IRQ*	P1-6
SIR	P1-32
IOO	P1-20
IOG	P1-15
SCL/SCM	P1-16,14
ENF	P1-46
IAK	P1-10
CLF	P1-7
STC	P1-22
CLC	P1-21



NOTES:
1. ARROWS POINT FROM SOURCE SIGNAL TO RESULTANT SIGNAL.
2. • INDICATES LOGICAL "AND" FUNCTION.
3. BROKEN LINE INDICATES UNKNOWN INITIAL STATE.
4. ALL SIGNALS REFERENCED TO GROUND (TPI).
5. * INDICATES PRIVILEGED INTERRUPT FENCE OUTPUT SIGNAL.

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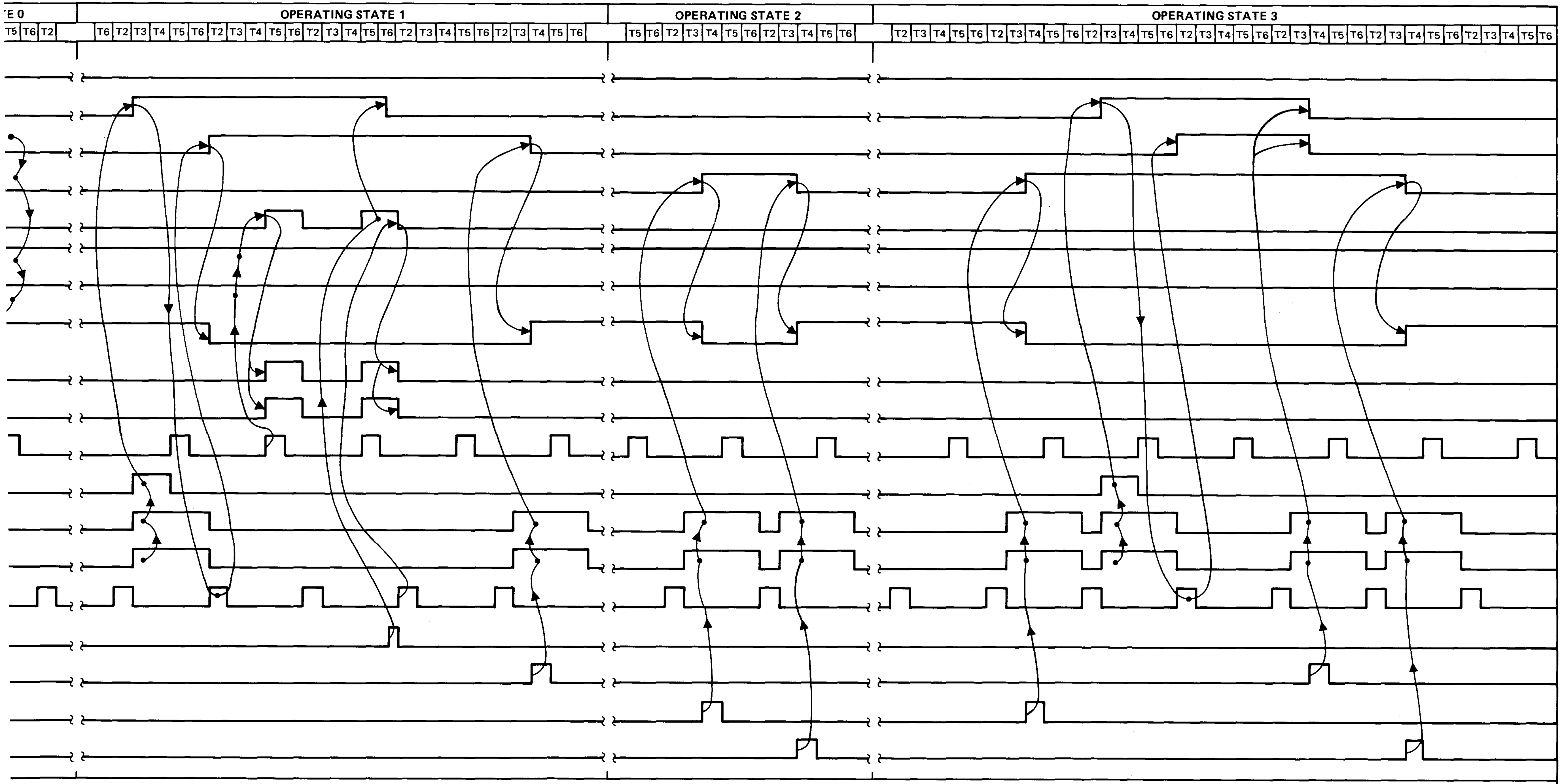
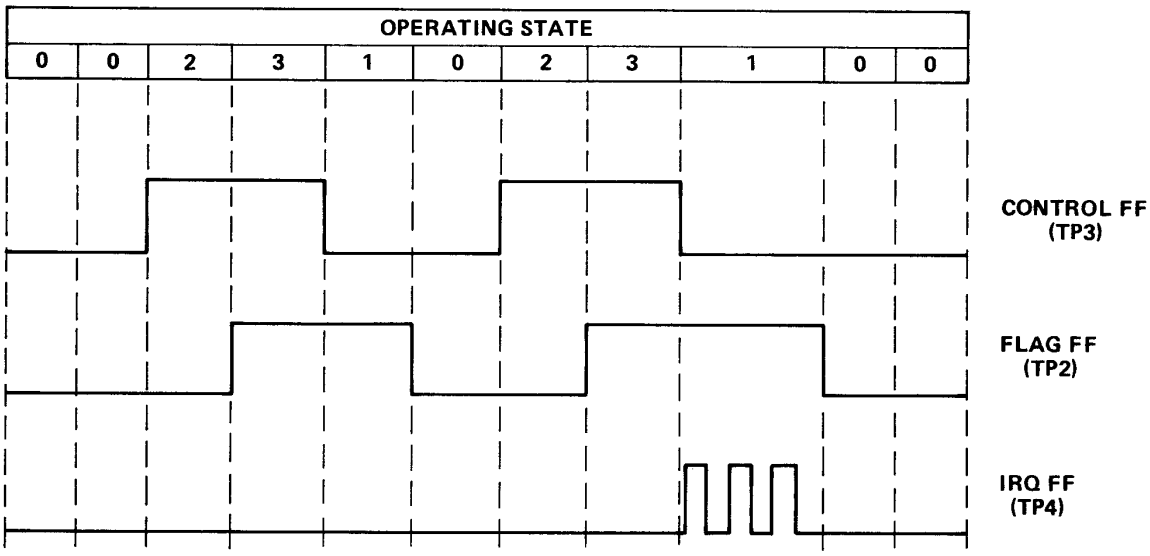


.TANT SIGNAL.

\TE.

4. ALL SIGNALS REFERENCED TO GROUND (TPI).
5. * INDICATES PRIVILEGED INTERRUPT FENCE OUTPUT SIGNAL.

Figure 2. Privileged Interrupt Fence Timing Diagram



TEST 9 - SCOPE LOOP

	I/O INSTRUCTION		FUNCTION	OPERATING STATE
START	STC	FCH	Sets Control FF	2
	NOP			2
	OTA	FCH	Sets Flag FF	3
	NOP			3
	CLC	FCH	Clears Control FF	1
	NOP			1
	CLF	FCH	Clears Flag FF	0
	STF	0	Enables Interrupt System	0
	STC	FCH	Sets Control FF	2
	NOP			2
	OTA	FCH	Set Flag FF	3
	NOP			3
	CLC	FCH	Clears Control FF	1
	NOP			1
	CLF	FCH	Clears Flag FF	0
	CLF	0	Disables Interrupt System	0
	---	--	Jumps to START	

NOTES: 1. NOP's provide a small time delay between each I/O instruction.

2. All waveforms are referenced to ground (TP1).

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Figure 3. Troubleshooting Waveforms

43. REPLACEABLE PARTS.

44. Table 4 provides a list, in reference designation order, for the replaceable parts for the HP 12936A Privileged Interrupt Fence. This table provides the following information for each part:

a. REFERENCE DESIGNATION. The reference designation for each replaceable part.

b. HP PART NO. The HP part number for each replaceable part.

c. DESCRIPTION. The description of each replaceable part. Refer to table 6 for an explanation of those abbreviations used in the DESCRIPTION column.

d. MFG CODE. A five digit code that denotes a typical manufacturer of a part. Refer to table 5 for a listing of manufacturers that correspond to the codes.

e. MFG PART NO. The manufacturer's part number for each replaceable part.

f. TQ. The total quantity of a part used on the PCA.

45. SHIPPING AND STORAGE.

46. If this accessory is to be shipped to Hewlett-Packard for service or repair, attach a tag to it identifying the owner and indicating the service or repair to be accomplished. Include the part number.

47. Package the PCA in the original factory packaging material, if available. If the original packaging is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Servide Office.

48. If standard factory packaging material is not used, wrap the PCA in Air Cap TH-240 cushioning (or an equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note: In any correspondence, identify the accessory by part number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

49. If this accessory is to be stored before use, package it as previously described to prevent accidental damage.

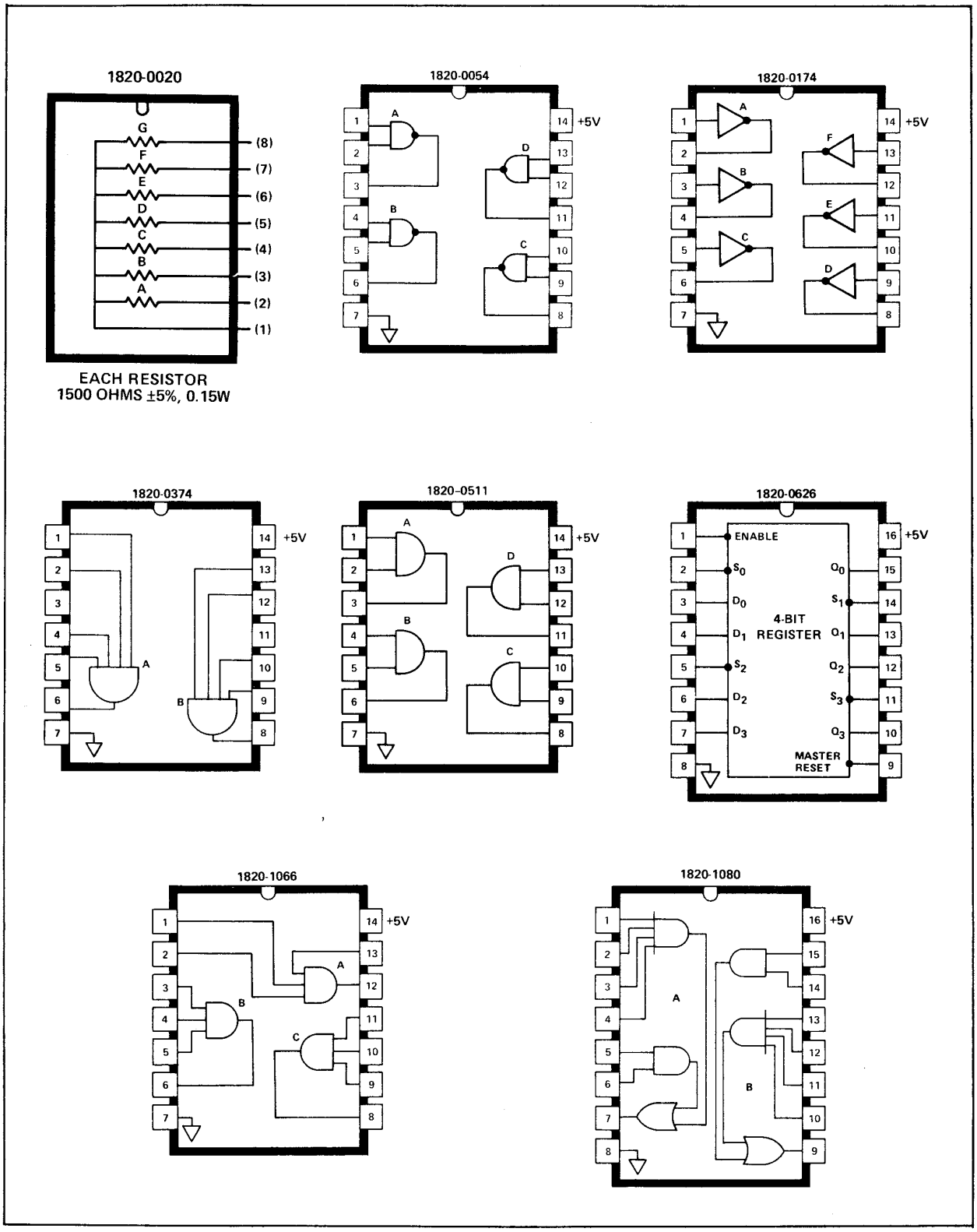

Figure 4. Integrated Circuit Diagrams

Table 4. Privileged Interrupt Fence Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
C1,2,5	0160-2055	CAPACITOR, FXD, CER, 0.01 UF, +80 -20%, 100 VDCW	28480	0160-2055	3
C3,4	0180-0374	CAPACITOR, FXD, ELECT, 10 UF, 10% 20 VDCW	28480	0180-0374	2
R1	0683-8215	RESISTOR, FXD, CARBON COMP, 820 OHM 5%, 0.25W	01121	CB8215	1
R2	0683-3315	RESISTOR, FXD, COMP, 330 OHMS, 5%, 1/4W	01121	CB3315	1
R3,4	1810-0020	RESISTOR, 7 x 1.5K OHMS, 5%, 500 PPM	56289	200C1098-CRR	2
U11,31	1820-0054	IC, QUAD 2-INPUT NAND GATE, TTL	01295	SN7400N	2
U13	1820-0374	IC, HS DUAL 4-INPUT AND GATE, TTL	01295	SN74H21N	1
U21	1820-1066	IC, TRIPLE 3-INPUT AND GATE, TTL	07263	U9A741159X	1
U23	1820-1080	IC, DGTL BUFFER, DRIVER, LINE DRIVER	18324	N8T13B	1
U33	1820-0511	IC, QUAD 2-INPUT AND GATE, TTL	01295	SN7408N	1
U41	1820-0174	IC, HEX INVERTER, TTL	01295	SN7404N	1
U43	1820-0626	IC, 4-BIT LATCH, TTL	07263	U7B931459X	1

Table 5. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
01121	Allen Bradley Co.	Milwaukee, Wis.	18324	Signetics Corp.	Sunnyvale, Cal.
01295	Texas Instruments, Inc. Transistor Products Division	Dallas, Texas	28480	Hewlett-Packard Co.	Palo Alto, Cal.
07263	Fairchild Camera & Instr. Corp., Semiconductor Division	Mountain View, Cal.	56289	Sprague Electric Co.	North Adams, Mass.

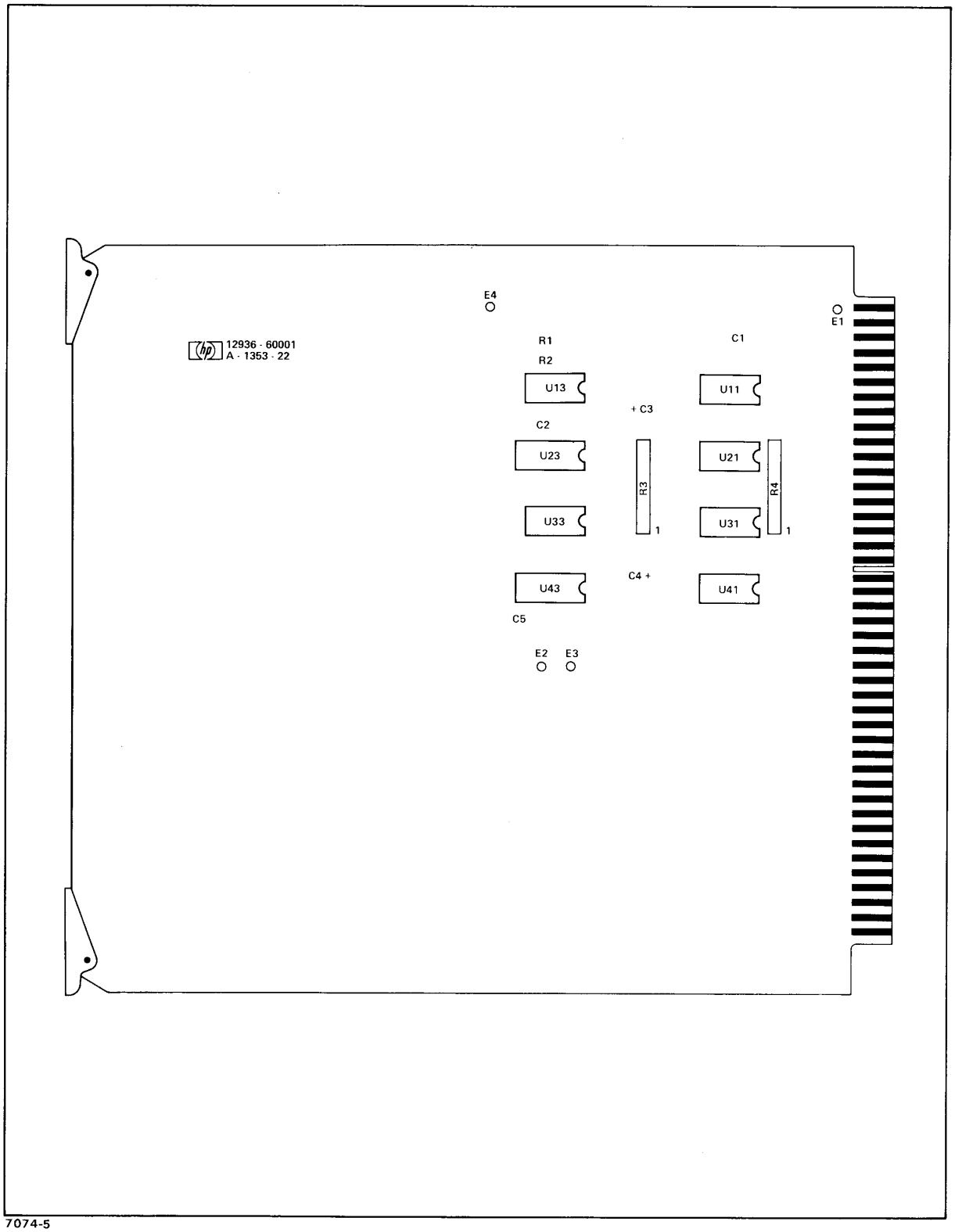

Figure 5. Privileged Interrupt Fence Parts Location Diagram

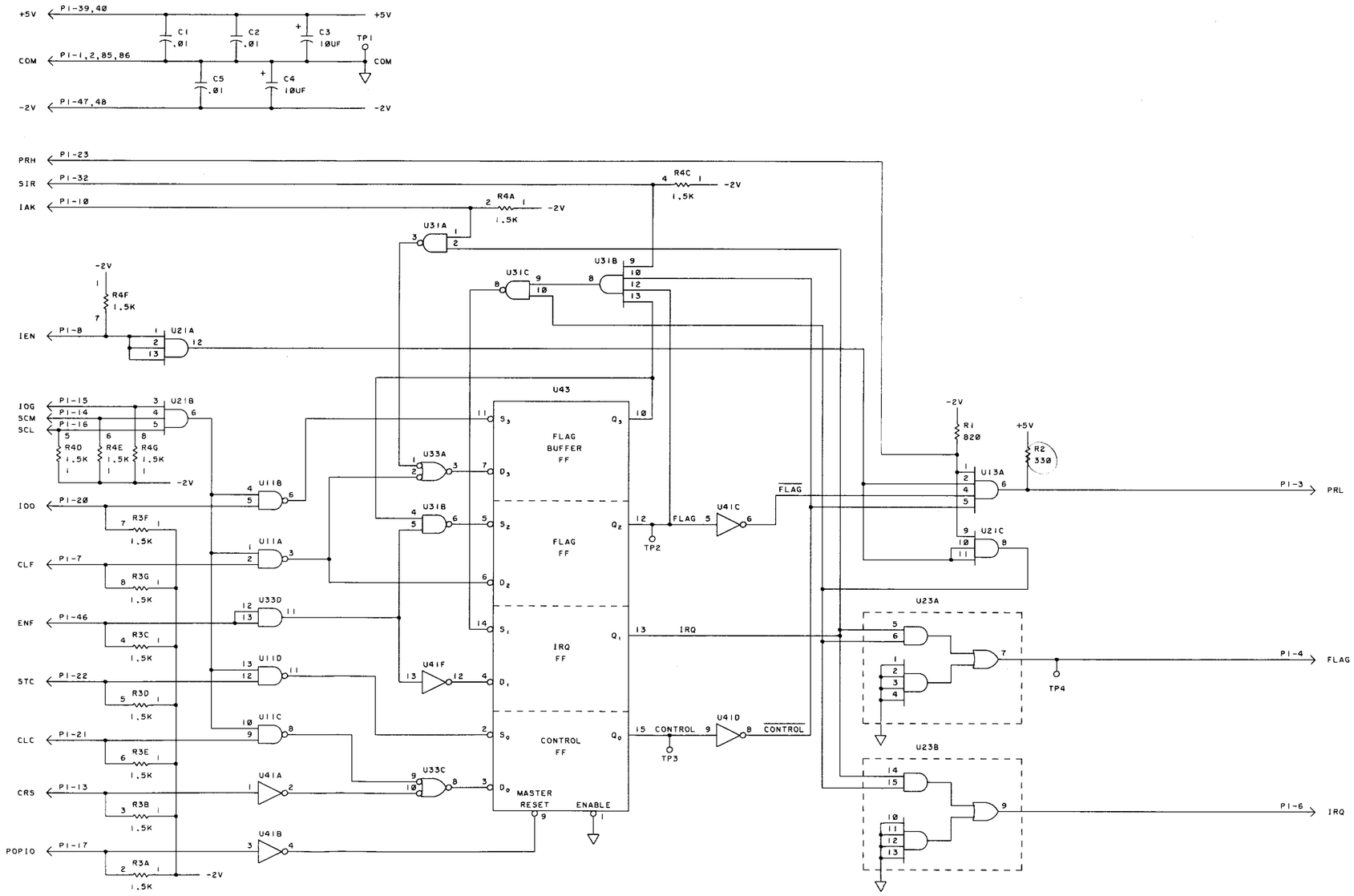

Figure 6. Privileged Interrupt Fence Schematic Diagram

APPENDIX A

HP 12936
Privileged Interrupt Fence Diagnostic

The HP 12936 Privileged Interrupt Fence Diagnostic confirms proper operation of the HP 12936 Privileged Interrupt Fence PCA (Printed-Circuit Assembly). This diagnostic is one of the 2100 series computer system diagnostics executed in conjunction with the HP 2100 Series Diagnostic Configurator. Test sequence and test failure reporting to the operator is provided through a teleprinter (if available), through the computer Memory Data Register (sometimes referred to as the MDR or T-register), and the A-register.

Operator input is required via the switch register for test options and via the A-register for individual test selection. The PRESET switch(es) are pressed by the operator to test the preset function.

The diagnostic consists of eight tests, which test all four functional states of the Privileged Interrupt Fence, and one troubleshooting scope loop.

GENERAL ENVIRONMENT

General hardware and software environments and system configuration procedures are described in the *HP 2100 Series Diagnostic Configurator (02100-90157).*

Hardware Requirement

1. The diagnostic is run on a 2100 series computer.

2. A paper tape reader is required to load the diagnostic only; the teleprinter paper tape reader can be used.

3. A system console teleprinter is optional, but recommended, to report error messages.

4. Two properly functioning I/O Interface PCAs (Printed-Circuit Assemblies) are required; they may be the teleprinter and the tape reader Interface PCAs.

   Note: If the Teleprinter Interface PCA is used, no test looping may be performed. Looping results in causing the teleprinter to chatter because CONTROL and FLAG are being set and cleared constantly.

5. The HP 12936 Privileged Interrupt Fence PCA is required.

6. I/O jumpers must be installed to effect unbroken priority.

Software Requirement

Required software consists of the following binary object tapes:

1. HP 2100 Series Diagnostic Configurator (HP 24296).

2. Privileged Interrupt Fence Diagnostic (HP 12936-16001).

Since the two I/O interface PCA's must be in working order, it is recommended that diagnostics, which correspond to each PCA, be executed prior to running the Privileged Interrupt Fence Diagnostic.

Loading is performed using the Binary Loader (usually memory resident). See the appropriate *Front Panel Procedures* for the 2100 series computer being used for use of the Binary Loader. The loader is described in the HP manual *Basic Binary Loader — Basic Binary Disc Loader — Basic Moving Head Disc Loader (HP 5951-1376).*

Operating Procedures

The Operating Procedures section is divided into four parts: Summary, Preparation for Diagnostic Run, Running the Diagnostic, and Diagnostic Messages and Halts.

SUMMARY

1. Load the configured Privileged Interrupt Fence Diagnostic using BBL, BBDL, or BMDL. If no configured binary tape of the diagnostic is available, refer to "Preparation for Diagnostic Run."

2. Set switch register = high and low interface select codes:

   bits 0 - 5 = low interface select code

   bits 6 - 11 = high interface select code

3. Set P-register = 100_8. Press PRESET (EXTERNAL PRESET and INTERNAL PRESET, if applicable); press RUN.

   Result: HALT

   - MDR = 102070_8 if valid SC (SC>7)
   - MDR = 102071_8 if lower SC is invalid
   - MDR = 102072_8 if higher SC is invalid

   If either select code is invalid, enter valid select code; press RUN.

4. Set bits 0-5 of switch register = the select code of the Privileged Interrupt Fence PCA; press RUN.

   Result: HALT

   - MDR = 102074_8 if valid SC
   - MDR = 102073_8 if invalid SC

   If select code is invalid, enter valid select code (SC>7) and press RUN.

5. Set the switch register = the program options (selected from Table 1); press RUN.

   Result: The message

   12936 PRIVILEGED INTERRUPT CARD DIAGNOSTIC

   is printed. Automatic execution of all selected tests begins.

   Note: If no teleprinter is available, test progress and results have to be monitored by MDR Halt codes. Refer to Table 2 for diagnostic messages that correspond to Halt codes.

   The message

   H032 PRESS PRESET (EXT), RUN

   is printed, if switch register bits 8 and 12 are clear.

6. If message H032 is printed, press PRESET (EXTERNAL PRESET, if applicable) and press RUN.

   Result: The diagnostic proceeds to completion, at which time the message

   PASS *nnnnnn*

   is printed, where *nnnnnn* is the octal pass count. A Halt follows with MDR = 102077_8 and the pass count in the A-register.

7. See section "Restarting Diagnostic," for diagnostic restart procedures.

PREPARE TO RUN THE DIAGNOSTIC

Before the tests can be initiated, the user performs the following:

1. Verify Proper Installation

   Install the Privileged Interrupt Fence PCA between two I/O Interface PCAs with interrupt capability. Insure that priority jumpers are installed to enable the priority string. The two I/O Interface PCAs must be error-free for valid Interrupt Fence diagnostic results.

   This diagnostic exercises the interrupt circuitry of the I/O Interface PCAs.

2. Load and Configure the Diagnostic Configurator

   Load the Diagnostic Configurator using the Binary Loader. Configuration instructions are found in the manual *Diagnostic Configurator (02100-90157)*. The teleprinter, optionally configured as the *System Output B Device*, is the only configuration parameter required for this diagnostic. All other configuration parameters are set to zero.

3. Load the Diagnostic

   Load the HP 12936 Privileged Interrupt Fence Diagnostic using the Binary Loader. The user may verify that the proper diagnostic is loaded by checking memory location 126_8 for the Diagnostic Serial Number = 103015_8.

4. Dump the Configuration (Optional)

   Using procedures described in the *Diagnostic Configurator* manual, the user may punch configured memory onto paper tape so that the above configuration procedures need not be repeated.

RUNNING THE DIAGNOSTIC

Parameter Entry and Program Options

Table 1 holds a summary of switch register options.

If *switch register bit 9* is set, either prior to starting test execution or while running, the diagnostic halts with MDR = 102075_8. The user then selects test *i* to be executed by setting bit *i* of the A-register. Refer to the first page of "Test Sections" for test section names and numbers.

Table 1. Switch Register Options

Bits	Function If Set
0 to 7	Reserved.
8	Suppress test 3 (operator intervention required).
9	Abort current tests; halt with MDR = 102075_8; user sets bits of A-register with test selection where bit *i* selects test *i*; e.g. bit 0 set selects test 0, bit 1 set selects test 1, etc. All tests are executed if A-register is clear.
10	Suppress printing of H-type messages (see Table 2).
11	Suppress printing of E-type messages (see Table 2).

Table 1. Switch Register Options (Continued)

Bits	Function If Set
12	Repeat all selected tests of diagnostic except test 3 (operator intervention is required in test 3) without executing a halt; the message "PASS *nnnnnn*" is printed at the end of each loop.
13	Repeat currently executing test (loop).
14	Suppress error halts (see Table 2).
15	Halt at the end of each test; MDR = 102076_8; A-register contains octal test just executed.

Restarting the Diagnostic

- To repeat the diagnostic as configured, press RUN.
- To change only the set of tests executed, do the following:
  1. Set bit 9 of switch register.
  2. Press RUN; a halt (MDR = 102075_8) results.
  3. Set A-register bits for tests desired (A-register clear means all tests are executed).
- To restart diagnostic anytime without any parameter change, do the following:
  1. Set P-register = 2000_8.
  2. Press PRESET (EXTERNAL PRESET and INTERNAL PRESET, if applicable).
  3. Press RUN.
- To restart diagnostic with new select codes, follow the procedure in the section "Summary."

DIAGNOSTIC MESSAGES AND HALTS

The diagnostic communicates to the operator through the teleprinter, halts, or both, based on configuration and switch register settings. Thus messages consist of halt codes (MDR and A-register values) and/or teleprinter text.

There are two general categories of messages output to the operator: program/operator communication messages and test failure (error) messages. Table 2 lists messages and halt codes. Messages coded with the letter "H" identify them as communication messages. All error messages are coded with the letter "E".

The test that outputs each message is indicated in the table. The tests are described in this manual under the heading "Test Sections."

"TC" refers to the Test Control routine.

"CF" refers to the select code configuration routine contained in this diagnostic.

Table 2. Messages and Halt Codes

Octal MDR Halt Code	Message	Test	Meaning
102070	–	CF	Select codes entered for high and low channel are valid; enter Privileged Interrupt Fence select code into switch register bits 0 to 5; press RUN.
102071	–	CF	Select code entered for high channel is invalid; reenter high and low select codes (SC>7) into switch register; press RUN.
102072	–	CF	Select code entered for low channel is invalid; reenter high and low select codes (SC>7) into switch register; press RUN.
102073	–	CF	Select code of Privileged Interrupt Fence was invalid; reenter valid select code (SC>7); press RUN.
102074	–	CF	Select code of Privileged Interrupt Fence was valid; enter program options into switch register (see Table 1); press RUN.

Table 2. Messages and Halt Codes (Continued)

Octal MDR Halt Code	Message	Test	Meaning
102075	–	TC	Test select halt which resulted from switch 9 being set; enter selection of tests to be executed into A-register; set bit *i* to select test *i*; A-register = 0 selects *all* tests to be executed.
102076	–	TC	End of test section halt resulting from switch 15 being set; A-register holds test section number just completed; press RUN to begin next test section.
–	12936 PRIVILEGED INTERRUPT CARD DIAGNOSTIC	TC	Introductory message.
–	TEST *nn*	TC	Indicates to which test a list of error messages, which follow, belongs; *nn* = test number.
102077	PASS *nnnnnn*	TC	All selected test sections of the diagnostic have completed; *nnnnnn* is the octal number of passes completed and is contained in the A-register, if the halt is invoked (switch 12 clear).
106077	–	TC	Halt stored in CPU memory locations 2_8 to 77_8 to trap interrupts which occur unexpectedly because of hardware malfunctions; M-register contains the I/O slot which interrupted; correct problem and reload diagnostic before continuing with diagnostic.
102030	E030 CLC CH FAILED TO CLEAR CONTROL OR PRIORITY CHAIN BROKEN	2	The Clear Control I/O instruction failed to clear the fence CONTROL; the fence was set to deny priority to the low channel; the CLC instruction execution should have allowed the low channel to interrupt.
102031	E031 CLC CH CAUSED FLAG TO SET	2	The CLC instruction resulted in setting the fence FLAG as well as clearing fence CONTROL; this caused the fence to interrupt erroneously.

Table 2. Messages and Halt Codes (Continued)

Octal MDR Halt Code	Message	Test	Meaning
102032	H032 PRESS PRESET (EXT), RUN	3	Press PRESET (EXTERNAL PRESET); press RUN.
102033	E033 PRESET (EXT) FAILED TO CLEAR CONTROL AND-OR FLAG OR PRIORITY CHAIN BROKEN	3	The PRESET (EXTERNAL PRESET) failed to clear fence CONTROL and/or its FLAG; the low channel is set to interrupt but is also denied priority while the fence CONTROL and FLAG are set; if PRESET clears the FLAG and CONTROL, the low channel should interrupt unless the priority chain is broken.
102034	E034 FENCE INT'D AFTER PRESET (EXT)	3	PRESET cleared CONTROL but not the fence FLAG; an erroneous interrupt resulted.
102035	E035 LOW CH SET TO INT BUT DID NOT INT	0	Low channel was set to interrupt but did not. Check the priority chain and the low channel PCA.
102036	E036 HI CH SET TO INT BUT DID NOT INT	1	High channel was set to interrupt but did not. Check the priority chain and the high channel PCA.
102040	E040 NO INT RECEIVED FROM LO OR HI CH	4	The high and low channels did not interrupt.
102041	E041 LO PRIORITY CH DID NOT INT AFTER HI	4	Low channel failed to interrupt after the high channel interrupted.
102042	E042 FENCE INT'D BEFORE HI CH BUT FENCE FLAG NOT SET	4	Fence should not interrupt but did interrupt before the high channel.
102043	E043 FENCE INT'D AFTER HI CH INT'D BUT FENCE FLAG NOT SET	4	Fence should not interrupt but did after high channel.
102044	E044 LO PRIORITY CH INT'D BEFORE HI CH	4	The low priority channel interrupted before the high priority channel.

Table 2. Messages and Halt Codes (Continued)

Octal MDR Halt Code	Message	Test	Meaning
102050	E050 NO INT RECEIVED FROM HI CH	5	The high and low channels are set to interrupt, but only the high channel should interrupt because the fence is up; no interrupt was received from high channel.
102051	E051 FENCE INT'D BEFORE HI CH BUT FENCE CONTROL SET	5	Fence should not interrupt but did interrupt before high channel.
102052	E052 FENCE INT'D AFTER HI CH INT'D BUT FENCE CONTROL SET	5	Fence should not interrupt but did interrupt after the high channel.
102053	E053 HI CH DID NOT INT BUT LO CH INT'D WITH FENCE UP	5	Low channel should not interrupt but did interrupt before high channel.
102054	E054 LO CH INT'D AFTER HI CH INT'D BUT FENCE UP	5	Low channel should not interrupt but did interrupt after high channel.
102060	E060 NO INT RECEIVED FROM HI CH	6	The high and low channels are set to interrupt while the Fence FLAG and Fence CONTROL are set; only the high channel should interrupt since the Fence is up; but the high channel did not interrupt.
102061	E061 FENCE INT'D BEFORE HI CH BUT FENCE FLAG AND CONTROL SET	6	Fence should not interrupt but did interrupt before the high channel.
102062	E062 FENCE INT'D AFTER HI CH INT'D BUT FLAG AND CONTROL SET	6	Fence should not interrupt but did after the high channel.
102063	E063 HI CH DID NOT INT BUT LO CH INT'D WITH FENCE UP	6	Low channel should not interrupt but did interrupt before the high channel.
102064	E064 LO CH INT'D AFTER HI CH INT'D BUT FENCE UP	6	Low channel should not interrupt but did interrupt after the high channel.

Table 2. Messages and Halt Codes (Continued)

Octal MDR Halt Code	Message	Test	Meaning
106000	E100 NO INT RECEIVED FROM FENCE OR LO CH	7	The low channel and fence are initially set to interrupt with the fence FLAG set and fence CONTROL clear; the fence should interrupt with low channel denied priority; if so, the high channel is set to interrupt and the fence FLAG cleared; the fence and low channel did not interrupt initially.
106001	E101 LO CH DID NOT INT AFTER HI CH	7	The low channel failed to interrupt after the high channel.
106002	E102 HI CH INT'D BEFORE FENCE	7	The high channel was not set to interrupt but did interrupt before the fence.
106003	E103 HI CH DID NOT INT AFTER THE FENCE	7	The high channel was set to interrupt after the fence but did not interrupt.
106004	E104 LO CH INT'D BUT FENCE AND HI CH DID NOT INT	7	Fence and high channel failed to interrupt, but low channel did interrupt; fence failed to deny priority to low channel.
106005	E105 LO CH INT'D AFTER FENCE INT'D BUT BEFORE HI CH INT'D	7	Low channel interrupted after the fence, but the high channel should have interrupted.
106010	E200 NO INT RECEIVED FROM FENCE OR HI CH	8	No interrupt was received when an interrupt was expected, first from the high channel, then from the fence.
106011	E201 FENCE DID NOT INT AFTER HI CH	8	The fence did not interrupt after the high channel interrupted.
106012	E202 FENCE INT'D BEFORE HI CH	8	The high channel should interrupt before the fence but the fence interrupted first.

Test Sections

The HP 12936 Privileged Interrupt Fence Diagnostic consists of nine test sections and a trouble-shooting loop section. The nine tests perform a go/no-go test of the Fence. When an error is detected, section 9 of the diagnostic, the scope loop, may be executed to observe FLAG, CONTROL, and IRQ states.

Testing of the Fence is based on the four states shown in figure 1 on page 3.

The tests provided by this diagnostic are:

Test	Function Tested
0	Low Priority Channel Interrupt
1	High Priority Channel Interrupt
2	Clear CONTROL
3	PRESET
4	No Action: FLAG and CONTROL cleared
5	Lower Priority: FLAG cleared and CONTROL set
6	Lower Priority: FLAG and CONTROL set
7	Lower Priority and Interrupt: FLAG set and CONTROL cleared
8	High/Fence Priority
9	Scope Loop

TEST 0 — LOW PRIORITY CHANNEL INTERRUPT

The ability of the low priority channel to interrupt is tested. The FLAG and CONTROL of the channel is set and the interrupt system turned on. The channel should interrupt but if it does not, error message E035 will occur.

TEST 1 — HIGH PRIORITY CHANNEL INTERRUPT

The ability of the high priority channel to interrupt is tested. The FLAG and CONTROL of the channel is set and the interrupt system turned on. The channel should interrupt but if it does not, error message E036 will occur.

TEST 2 — CLEAR CONTROL

The ability of the I/O instruction CLC FCH (FCH = fence channel) to clear fence CONTROL is tested. This is done by setting the low channel to interrupt and by setting the fence CONTROL and clearing the fence FLAG followed by turning on the interrupt system. With the fence CONTROL set and FLAG cleared, priority to the low channel should be denied. When the CLC FCH instruction is executed the fence CONTROL should clear, resulting in the low priority channel interrupting.

If the low channel does not interrupt, error message E030 will occur.

If the fence channel interrupts (fence FLAG and CONTROL set), error message E031 will occur.

TEST 3 — PRESET

The ability of EXTERNAL PRESET to clear the fence CONTROL and FLAG is tested. This is done by setting fence FLAG and CONTROL (lowers priority) followed by message H032.

When RUN is pressed, the program sets the low priority channel to interrupt and turns on the interrupt system. Since EXTERNAL PRESET clears fence FLAG and CONTROL, the low priority channel should interrupt.

If the low priority channel does not interrupt, error message E033 results.

If the fence CONTROL is cleared, but FLAG does not clear, then the fence will interrupt resulting in error message E034.

TEST 4 — NO ACTION: FLAG AND CONTROL CLEARED

This test checks that with the fence FLAG and CONTROL cleared that a lower priority channel is not denied priority and that the fence does not interrupt. This is done by setting the low and high priority channels to interrupt. If the card is functioning properly the high channel should interrupt, followed by the low channel.

If the low and high channel fail to interrupt, error message E040 results.

If the low channel fails to interrupt after the high channel, error message E043 results.

Finally if the low channel interrupts before the high channel, error message E044 results.

TEST 5 — LOWER PRIORITY: FLAG CLEARED AND CONTROL SET

This test checks that with the fence FLAG cleared and CONTROL set, that a low priority device may be denied priority while the high priority channel may still interrupt. This is done by setting the low and high channels to interrupt. If the card is functioning properly, only the high channel should interrupt.

If the high channel does not interrupt, error message E050 results.

If the fence interrupts before the high channel, error message E051 results.

If the fence interrupts after the high channel, error message E052 results.

If the low channel interrupts before the high channel, error message E053 results.

If the low channel interrupts after the high channel, error message E054 results.

TEST 6 — LOWER PRIORITY: FLAG AND CONTROL SET

This test is basically the same as test 5 with the only difference being the fence FLAG is set as well as the CONTROL.

If the high channel does not interrupt, error message E060 results.

If the fence interrupts before the high channel, error message E061 results.

If the fence interrupts after the high channel, error message E062 results.

If the low channel interrupts before the high channel, error message E063 results.

If the low channel interrupts after the high channel, error message E064 results.

TEST 7 — LOWER PRIORITY AND INTERRUPT: FLAG SET AND CONTROL CLEARED

This test checks that with the fence FLAG set and CONTROL cleared that the fence denies priority to a lower channel and that it will interrupt. This is done by initially setting the low channel and fence to interrupt. If the card is functioning properly, the fence will interrupt. If the fence interrupts properly the high channel is set to interrupt and the fence lowered. The high channel followed by the low channel should now interrupt.

If the fence or low channel fail to interrupt, error message E100 results.

If high channel fails to interrupt after fence, error message E103 results.

If the low channel fails to interrupt after the high channel, error message E101 results.

If the high channel interrupts before the fence, error message E102 results.

If the low channel interrupts before either the fence or high channel interrupts, error message E104 results.

If the low channel interrupts after the fence interrupts, but before the high channels interrupts, error message E105 results.

TEST 8 — HIGH/FENCE PRIORITY

This test checks that with the fence FLAG and CONTROL set that the high channel can deny priority to the fence. If the card is functioning properly the high channel should interrupt followed by the fence.

If the fence or low channel fail to interrupt, error message E200 results.

If the fence fails to interrupt after the high channel, error message E201 results.

If the fence interrupts before the high channel, error message E202 results.

TEST 9 — SCOPE LOOP

This section provides a scope loop on the fence card. The loop consists of the following sequence of I/O instructions.

```
STC   FCH      set control
OTA   FCH      set flag
CLC   FCH      clear control
CLF   FCH      clear flag
STF   0        turn on int system
STC   FCH      set control
OTA   FCH      set flag
CLC   FCH      clear control
CLF   FCH      clear flag
CLF   0        turn off int system
(loop to first instruction)
```

A small time delay precedes each I/O instruction. To exit this loop, bit 9 of switch register is set followed by clearing bit 9 of A-register.

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